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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,125	09/21/2001	Ciaran Gerard O'Donnell	US 018157	4203

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EXAMINER	
MYERS, PAUL R	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/961,125	O'DONNELL, CIARAN GERARD	
	Examiner	Art Unit	
	Paul R. Myers	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-4, 8-19, 21, 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yona et al PN 7,085,875 in view of Zou PN 6,160,796.

In regards to claims 1-2: Yona et al teaches a plurality of serial buses (22; Sub-busses of size N; when N=1 the sub-buses are serial) that is configured to provide interconnections among a plurality of cards, a bus allocation control unit that is configured to receive requests for bandwidth allocation from the plurality of cards (32), and to provide allocations of subsets of the plurality of serial buses to satisfy the requests (Abstract) wherein the bus allocation control unit aggregates multiple serial buses to satisfy a single request (Abstract). Yona et al does not teach his bandwidth control is in a Home control platform or expressly that the cards include processing units. While the examiner recognizes that the cards would inherently include processing units. Since Zou also expressly teaches processing units, this point is mute. Zou teaches a home control platform comprising a plurality of serial buses (30a-f) that are configured

to provide interconnection among a plurality of processing units (12, 14, 16, 18, 20, 22, 24), a bus allocation control unit (CMM 250) that is configured to receive requests for bandwidth allocation from the plurality of processing units, and to provide allocations of a subset of the plurality of serial buses to satisfy the request (Col. 9, lines 45-64). Zou does not expressly teach the control unit aggregates multiple serial buses to satisfy a singles bandwidth request. It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement Yona et al's bandwidth allocation control system in a home control network because this would have allowed greater bandwidth control in the home control network.

In regards to claim 3, Zou teaches at least one processing unit includes at least one of: an MPEG decoder, an MPEG encoder a signal processor, a variable-length decoder, a variable-length encoder, a coder-decoder, a video CODEC, an audio CODEC, a Fast-Fourier-Transform device, a Discrete-Cosine-Transform device, a video processor, and an audio processor (e.g. fig. 1; fig. 2; col. 2, lines 60-65).

In regards to claims 4, 10: Zou teaches at least one processing unit includes at least one of: a serial-to-parallel converter, a parallel-to-serial converter, a bus arbitrator, a bus router, and a direct-memory-access device (e.g. fig. 2; fig. 4; fig. 5A, 5B)

In regards to claim 8: Yona et al and Zou both teach at least one control processor (32 in Yona, DCM in Zou) that is configured to provide control of data transfer among the plurality of processing units.

In regards to claim 9: Yona et al teaches a network interface. Zou teaches the at least one control processor includes at least one of: a network interface, a network manager, a browser, and a user interface (col. 8, lines 30-31).

In regards to claim 11: Zou discloses the home control platform of claim 8, wherein the at least one control processor includes: a bus interface unit (fig. 2), operably coupled to the plurality of serial buses, that is configured to effect transfer of data via the plurality of serial buses, and a central processing unit (101), operably coupled to the bus interface unit, that is configured to process input data from the bus interface unit, and is configured to provide processed data to the bus interface unit (col. 8, lines 15-34).

In regards to claim 12: Zou discloses the home control platform of claim 11, wherein the at least one control processor further includes an SDRAM (memory; fig. 2).

In regards to claims 13, 26: Zou teaches the at least one control processor further includes a microkernel that is configured to provide base operating system services that include at least one of: semaphores, messaging, scheduling, exception management, task management, and memory management (col. 9, lines 5-67).

In regards to claims 14, 27: Zou teaches the at least one control processor further includes an interface that is configured to couple the microkernel to a standard operating system (col. 12, lines 1 et seq.; fig. 3; fig. 8).

In regards to claim 15: Zou discloses the home control platform of claim 14, wherein the standard operating system includes one of: Vxworks, WinCE, and LINUX (col. 8, lines 31 et seq.).

In regards to claims16, 28: Zou teaches the task management is configured to provide direct access to at least one of the plurality of processing units, the at least one of the plurality of processing units being configured as a coprocessor, and the direct access being provided through a coprocessor interface layer (col. 8, lines 1-67).

In regards to claim 17: Zou discloses the home control platform of claim 8, wherein the at least one control processor is further configured to provide at least one of: task memory and CPU space isolation, virus protection, and money management (col. 8, lines 15-29).

In regards to claims 18, 29: Zou teaches the at least one control processor is further configured to provide an interface between the home control platform and at least one legacy consumer product, the at least one legacy consumer product includes at least one of: a television, a telephone, an audio system, a video system, and an appliance (fig. 1A).

In regards to claims 19, 30: Zou teaches the at least one control processor includes at least one of: a voice recognition system, a voice synthesis system, and a wireless device interface system (e.g. CD system; fig. 1A).

In regards to claim 21: Both Yona et al and Zou inherently include a power supply that is configured to provide power to one or more of the plurality of units.

In regards to claim 25: Yona and Zou both teach a control processor (e.g. top-set-box) for use in a home control platform, comprising: a bus interface unit, operably coupled to a plurality of serial buses of the home control platform, that is configured to effect transfer of data via the plurality of serial buses (1394; 30a-f), based on an allocation of a select one or more buses of the plurality of serial buses by the home control platform (col. 9, lines 45-64), and a central processing unit, operably coupled to the bus interface unit, that is configured to process input data from the bus interface unit, and is configured to provide processed data to the bus interface unit (fig. 2).

4. Claims 5-7, 20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yona et al PN 7,085,875 in view of Zou PN 6,160,796 as applied to claim 1 above and further in view of Brotz et al. PN 6,374,404.

In regards to claim 5-7 and 20, Yona et al in view of Zou discloses the invention as applied to claim 1 above. Yona et al only teaches that the units are cards and not what the card are. Zou does not explicitly disclose at least one processing unit includes: a filter unit, and a SDRAM and wherein the filter unit is configured to be programmable; and wherein each of the plurality of serial buses is configured to be self-timing. Brotz, teaches a system of providing intelligent devices in a HAVI system, teach the use of an intelligent filter system (300) in a set-top-box (fig. 3) and a SDRAM (cache memory 102a) wherein the filter system 300 is

programmable to filter web pages (col. 2, lines 60-67; col. 9, lines 5-14). Brotz further teaches the use of self-timing bus (col. 11, lines 60 et seq. to col. 12, lines 1-14). It would have been obvious to one of ordinary skill in the home network system art at the time the invention was made to employ a programmable filtering system and memory in the HAVI system such as that of Zou as taught by Brotz. Brotz teaches that the a programmable filtering system and memory would allow users to cache the most frequently viewed web pages and would enable the system to update the user/viewer selections based on the behavior and viewing patterns/history of the user. With the provision of the cache memory 102e therefore increases the user's internet connectivity experience by eliminating any perceived latencies for selected web pages that are associated with a cache hit. (col. 10, lines 20-24).

As per claims 22-24, Zou discloses the claimed invention including a processing unit for use in a home control platform (e.g. figs. 1-2) comprising: a bus interface unit, processor and plurality of serial buses (1394; 30a-f). Zou does not disclose at least one processing unit includes: a filter unit, and a SDRAM and wherein the filter unit is configured to be programmable. Brotz, in the system of providing intelligent devices in a HAVI system, teach the use of an intelligent filter system (300) in a set-top-box (fig. 3) and a SDRAM (cache memory 102a) wherein the filter system 300 is programmable to filter web pages (col. 2, lines 60-67; col. 9, lines 5-14). Brotz further teaches the use of self-timing bus (col. 11, lines 60 et seq. to col. 12, lines 1-14). It would have been obvious to one of ordinary skill in the home network system art at the time the invention was made to employ a programmable filtering system and memory in the HAVI system such as that of Zou as taught by Brotz. Brotz teaches that the a programmable filtering system and memory would allow users to cache the most frequently viewed web pages

and would enable the system to update the user/viewer selections based on the behavior and viewing patterns/history of the user. With the provision of the cache memory 102e therefore increases the user's internet connectivity experience by eliminating any perceived latencies for selected web pages that are associated with a cache hit. (col. 10, lines 20-24).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PRM
January 25, 2007

PAUL R. MYERS
PRIMARY EXAMINER